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PATENT
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Applicant:	Chason et al.
Serial No.:	10/044,777
Filed:	January 11, 2002
Title:	SEMICONDUCTOR RACKAGE DEVICE AND METHOD
Group Art Unit:	2811
Examiner:	Jones, J.

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on this date.

7/17/02 Kelly Reese
Date

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Dear Sir:

This Information Disclosure Statement is being submitted in accordance with 37 C.F.R. §§1.97 - 1.98 in connection with the above-identified application. The following documents are listed below.

U.S. Patent Documents

Patent No.	Inventor(s)	Issue Date
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6,376,278	Egawa et al.	4/23/02
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6,297,560	Capote et al.	10/2/01
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6,238,223	Cobbley et al.	5/29/01
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6,132,646	Zhou et al.	10/17/00
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6,075,290	Schaefer et al.	6/13/00
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5,128,746	Pennisi et al.	7/7/92

U.S. Published Applications

Publication No.	**Publication Date**	**Inventor(s)**
US 2001/0012680 A1	August 9, 2001	Cobbley et al.
US 2002/0014703 A1	February 7, 2002	Capote et al.

Foreign Patent Documents

Document No.	Country	Publication Date
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Mr. Albert Capote et al., *"A Novel Flip-Scale package Using Pre-Applied Multilayer Flip-Chip Under-Encapsulation,"* Pan Pacific Microelectronics Symposium pg. 153-158 (1999)

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The above items are listed on Form PTO-SB-08A which accompanies this Information Disclosure Statement. A copy of each document cited thereon is enclosed herewith.

Pursuant to 37 CFR §1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR § 1.56(b).

The Commissioner is hereby authorized to charge any additional fees which may be required in this application to Deposit Account No. 06-1135.

Respectfully submitted,
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